Abstract of the Disclosure

A method and apparatus of reducing the time for enabling a dynamic random access memory (DRAM) upon initial application of power, comprises generating an internal RAS signal upon initial power up to generate internal voltages. The internal RAS pulse is asserted after a short time delay ends. After the internal RAS pulse is asserted, voltages on a digit line pair are amplified with a sense amplifier. Then, the amplified voltages on the digit line pair are equilibrated with an equilibration circuit. The equilibrated voltage is also coupled through the equilibration circuit to charge a common plate of a memory cell capacitor.

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